block diagram of the interrupt control section.

When an interrupt signal is received, data in the program counter, accumulators A and B, and condition code register are saved automatically in the RAM as indicated by the stack pointer, and are restored through the return instruction from the interrupt. Data in the index registers are saved under software control because a careful review of various software indicated that when the data in the index registers are automatically saved, RAM efficiency is lowered. The interrupt overhead including the register data save operation is only 5 µsec.

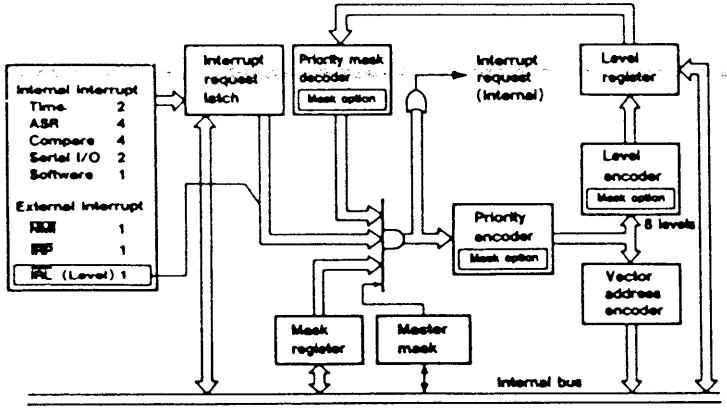

Fig. 11 - Block diagram of interrupt control section

General Purpose Input/Output Ports

There are two 8-bit input/output ports, A and B. In the single-chip mode, they function as input/output ports, while in the external bus mode they function for address bus (port A) and address/data bus (port B). Data direction registers are installed for ports A and B in

inputs for detecting/recording the event occurrence time
- four 16-bit compare registers for establishing the comparison time with the above-mentioned timer, and the synchronization detection circuit
- a 6-bit output port giving signals with the above-mentioned synchronized timing or by the software

The timer counter is a 18-bit counter which is incremented every 1 µsec when the crystal oscillator frequency is 12 MHz. It outputs counter overflow interrupt requests every 262 msec and 4/2/1/0.125 msec interval interrupt requests selected by the program. Reading of the timer counter by the program is usually from high-order 16 bits.

The ASR registers automatically latch timer counter values at the event occurrence (leading and/or trailing edges) of corresponding input terminals. These hardware pieces have made it possible to measure pulse durations and frequencies with a high degree of accuracy without software assistance.

ASR0 and ASR1 each consists of a pair of 16-bit ASR registers, which record the rise and fall timing of input signals of each channel with 1 µsec resolution. ASR3 and ASR4 are 4 µsec resolution ASR registers, whose input signal edge selection (leading and trailing) is assigned by the software. An interrupt request signal indicating an event occurrence is generated at each channel.

Data written in each of the four compare registers are always compared with the high-order 16 bits value of the timer counter. When they become identical, an interrupt request signal corresponding to each compare register is generated. This identification signal is used as the data read timing of the digital output DOUT latch, whereby any 4 µsec resolution pulse signal may be generated.