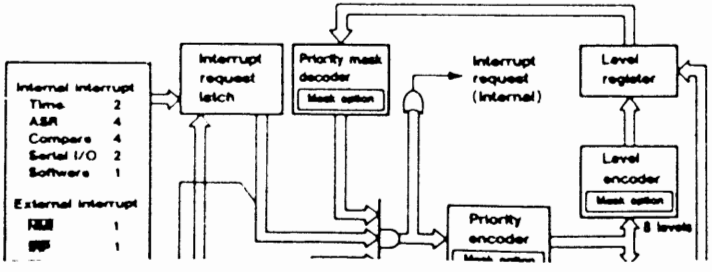
Interrupt Control Function

The CPU has a powerful multiple interrupt function for the high-speed I/O processing. A total of 12 input interrupt signals are possible: two interrupt signals from the timer counter, four each from both the ASR registers (discussed below) and the compare registers, and two serial I/O interrupt signals for the interruption from the internal I/O. External interrupts include a non-maskable interrupt (NMI), an edge input (IRP), and a level input (IRL). In addition, a software interrupt is available; a total of 16 interrupt factors are therefore possible.

Interrupt priority is given at eight levels. Each interrupt can be assigned to an arbitrary priority level through the mask option of the mask ROM stage. At the same time, priorities may be similarly designated through the mask option when multiple demands exist within one level. This flexible optional function makes it possible for various engine control systems to operate under optimum conditions. Figure 11 shows a block diagram of the interrupt control section.

When an interrupt signal is received, data in the program counter, accumulators A and B, and condition code register are saved automatically in the RAM as indicated by the stack pointer, and are restored through the return instruction from the interrupt. Data in the index registers are saved under software control because a careful review of various software indicated that when the data in the index registers are automatically saved, RAM efficiency is lowered. The interrupt overhead including the register data save operation is only 5 µsec.



order to designate bit-unit input and output in the single-chip mode. In addition, four of the terminals of port A are equipped with a leading/trailing edge detection function as well as a 4-bit flag register. These ports may be used for other purposes such as switch-input/level-output not requiring high-speed processing. Further, port B can be used as an input port with a strobing function by IS signals, making it possible to achieve an 8-bit data handshake with other systems in combination with IS (Input Strobe) interrupt and OS (Output Strobe) signals.

High-Speed I/O

The CPU has several powerful timer-based high-speed I/O's, which can independently measure the input timing and the output timing of pulse signals. Figure 12 shows the block diagram of the high-speed I/O section.

- a 18-bit, free-running counter with 1 µsec resolution
- six 16-bit ASRs (Auto Save Registers) with 4 inputs for detecting/recording the event occurrence time
- four 16-bit compare registers for establishing the comparison time with the above-mentioned timer, and the synchronization detection circuit
- a 6-bit output port giving signals with the above-mentioned synchronized timing or by the software

The timer counter is a 18-bit counter which is incremented every 1 µsec when the crystal oscillator frequency is 12 MHz. It outputs counter overflow interrupt requests every 262 msec and 4/2/1/0.125 msec interval interrupt requests selected by the program. Reading of the timer counter by the program is usually from high-order 16 bits.

The ASR registers automatically latch timer counter values at the event occurrence (leading and/or trailing edges) of corresponding input terminals. These hardware pieces have made it possible to measure pulse durations and frequencies with a high degree of accuracy without software assistance.

ASR0 and ASR1 each consists of a pair of