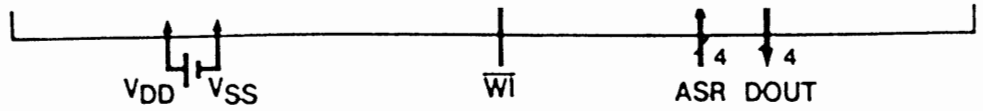

Fig. 9 - CPU block diagram

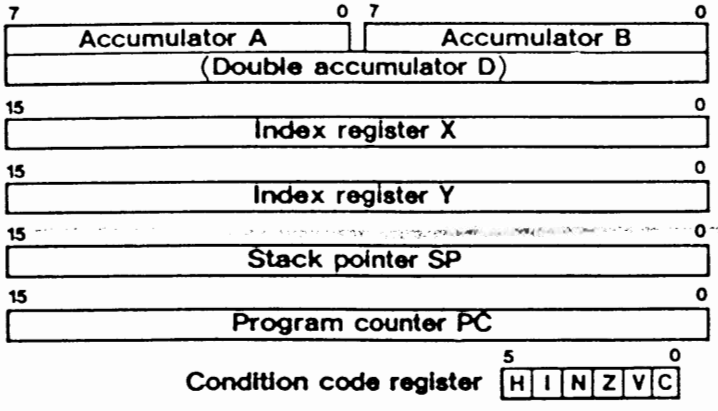

Fig. 10 - Internal registers

Instruction Set

The instruction set of the single-chip microcomputer effectively performs instructions for automotive application, making it easy to develop software and to improve the processing speed and memory efficiency. There are 255 instructions including addressable multiplication and division instructions, a number of bit manipulation instructions, direct operation instructions to the memory and I/O registers, inter-register transfer instructions, and double-byte instructions.

There are nine addressing modes, which are factors accessible to the memory:

- IMMEDIATE
- INDEXED
- RELATIVE
- INDIRECT
- DIRECT FOR ACCESS TO ADDRESSES 0-255
- EXTENDED FOR ACCESS TO 64K bytes
- INHERENT WITHOUT OPERAND
- MEMORY IMMEDIATE FOR DIRECT OPERATION TO ADDRESSES 0-255
- BIT MANIPULATION TO ADDRESSES 32-47 AND 64-79

Internal Memory and Memory Connection Function

Memory capacity is an 8K-byte user ROM, a 256-byte RAM (of which 32/64 bytes may be used as a stand-by RAM), and a 256-byte test ROM. The test ROM is included in order to improve the testing and screening efficiency of the CPU, and is used only when the CPU is shipped. Usually at the time of mass production, the engine control system is used in the single-chip mode operating in accordance with the control program stored in the internal memory of the CPU, however the external bus mode may also be selected for the software development and system expansion. Address expansion is possible up to 64K bytes in this case. Universal type memory chips and peripheral I/O chips may be connected without interface.