

the context switch function has reduced interrupt overhead time to a mere 2.5 μ sec.

Instruction Set

The instruction set for this microcomputer is a superset of the M68000 instruction set.

Six new instructions have been added to specifically address the requirements of this automotive application. Four of these instructions (SETB, CLRB, BRSET, BRCLR) are bit operation instructions and have been widely used in the previous and current 8-bit microcomputer solutions. In the current engine control applications, these instructions often represent 15 to 20 percent of the total number of instructions in a given program.

Without these instructions, use of a similar programming approach could increase the size of program memory by as much as 10 to 15 percent. The instructions were included such that programming techniques and application code proven with 8-bit solutions could continue to be applied with minimal execution time and efficient use of program memory. The other two instructions (MOVEC and MOVEAX) support access to the context switch control register (used in managing the two register sets) and enable execution of 32-bit transfers between CPU registers and onboard RAM, respectively.

Memory

This microcomputer contains 45 KB user ROM and 2 KB user RAM. The majority of the engine control systems currently in mass production are configured with 12 KB of ROM, and that of the transmission control systems are configured with 6 KB of ROM. Thus this microcomputer leaves a considerable amount of space to add new functions. Up to 0.5 KB of RAM can be used as standby RAM.

independently. Two full duplex transmission modes are provided, i. e., an asynchronous mode and a synchronous mode. Two check functions have been added to increase the reliability of received data and to ensure that no malfunctions have occurred due to noise. Furthermore, data can be transmitted with the SIO reception or transmission area using the DMA function described above.

Serial Extension Interface (SEI)

SEI is used for serial transmission between independent peripheral devices. Fig. 6 shows an example of the interface used with an external A/D converter. When the SEI is informed via the end of conversion (EOC) line that the A/D conversion has been completed, data is moved from the buffer register to the shift register, and the shift is commenced. The shift clock is output in 16 bits, the same length as data, from SCLK, and data are transmitted in a synchronized manner. This is issued as a command to the A/D converter, and at the same time, the last converted data is transferred to the shift register. When the 16-bit data transmission has been completed,

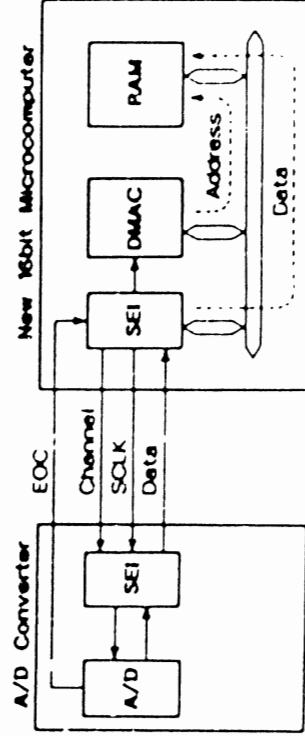


Fig. 6 Communication with A/D Converter